Virtual Platforms for the ORCA Chip Architecture: A Comparative Analysis

Melvin Galicia[(1)], Daniel Keßel[(2)], André Zambanini[(2)], Rainer Leupers[(1)] and Stefan van Waasen[(2)]

[(1)] RWTH Aachen University - Software Systems on Silicon (ICE),

[(2)] Forschungszentrum Jülich - Integrated Computing Architectures (ICA | PGI-4)

There is growing demand for virtual platforms capable of modeling the functionality, timing, and power consumption of components integrated within complex systems, including those that incorporate neuromorphic accelerators. This demand stems from their value in simulating how artificial neural network applications execute on architecture-specific neuromorphic hardware, such as the ORCA chip planned in the NEUROTEC II[1] project shown in Figure 1.

These virtual platforms can be implemented using different approaches to evaluate performance and energy efficiency at the electronic system level (ESL). Two approaches have been explored and implemented: a bottom-up SystemC methodology [1] and a top-down gem5 modular platform [2]. Both SystemC and gem5 are employed in academia and industry for early architecture exploration. Our contribution will compare their respective advantages and disadvantages, highlighting how each approach supports different stages of system-level modeling and evaluation.

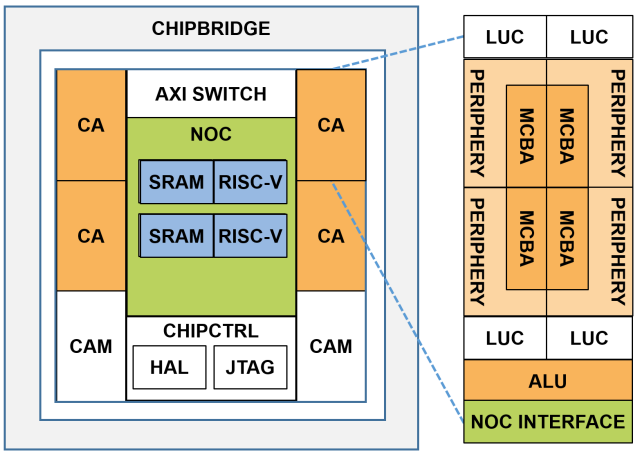

Figure 1: ORCA chip architecture. The two approaches include: RISC-V processors and SRAM, network-on-chip (NOC), neuromorphic accelerators (Compute Arrays (CAs)) and memristive crossbar arrays (MCBAs) for compute-in-memory (Colors for visualization only)

SystemC native approach: SystemC is a widely used, ISO-standardized C++ class library for system and hardware design. The advantages of this include plenty of literature support, modification flexibility and debugging tools. One disadvantage is that the bottom-up approach requires most components to be built and modeled from scratch. The simulation platform developed in [1] allowed for the verification of power and performance estimation results at the ESL modeling, including instruction tracing, while facilitating rapid design space exploration.

gem5 approach: gem5 is a modular open-source simulator for computer system architectures, written in C++. It is a popular choice because of its included models for CPUs, networks, GPUs, and more. It uses a standardized interface for components to connect, allowing easy architectural exploration through the replacement of single components. This also allows a straightforward top-down approach where components can initially be modeled with basic functionalities and then gradually extended with new functions or more accurate simulations. One disadvantage of gem5 is that it is a monolithic repository, instead of a set of libraries. Included components may therefore be overly specialized, necessitating adapted versions for correct ORCA simulation. These were explored in [2].

[1] M. Galicia et al., "NeuroVP: A System-Level Virtual Platform for Integration of Neuromorphic Accelerators," 2021 IEEE 34th International System-on-Chip Conference (SOCC), Las Vegas, NV, USA, 2021, pp. 236-241.

[2] D. Keßel, "System-Level Simulation of Neuromorphic Hardware Accelerators in gem5". Master's thesis, RWTH Aachen University, 2025.

[1]NEUROTEC II is supported by the German Federal Ministry of Research, Technology and Space (BMFTR) with grant numbers 16ME0398K and 16ME0399.